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2662

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	09/737375	Docket Number	MIPS.0164-01-US
Filed	12/14/00	Group Art Unit	2662
Examiner	GREGORY B. SEFCHECK	Customer No.	23669
Application Title	QUEUEING SYSTEM FOR PROCESSORS IN PACKET ROUTING OPERATIONS		
First Named Inventor	MARIO D. NEMIROVSKY		

INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Attached hereto is Form PTO-1449, submitted under 37 CFR 1.97(d) and 1.97(e)(2), listing documents believed relevant to the subject application. It is respectfully requested that the examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims and return an initialed copy of each form to the undersigned.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 CFR 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b) or is available as a reference under 35 U.S.C. §102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the allege "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 CFR 1.56, 1.97 and 1.98, and the Manual of Patent Examining Procedures § 609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

The enclosed documents may have markings thereon. No significance is intended to be attached to the markings.

No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. The information cited in the information disclosure statement was cited by the United States Patent Office in one or more applications that are related to the present application.

02/03/2005 DBERAKX1 00000016 09737375

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Application No. 09/737375 (Docket: MIPS.0164-01-US)
Information Disclosure Statement Transmittal dated 1/28/05

Also attached hereto is the fee for submission of an IDS in the amount of **\$180.00** as forth in § 1.17(p).

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I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop **AMENDMENT**, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

By


RICHARD K. HUFFMAN

Reg. No. 41,082

Tel.: (719) 575-9998

Date

1/28/05





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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
				Application Number	09/737375
				Filing Date	12/14/00
				First Named Inventor	MARIO D. NEMIROVSKY
				Group Art Unit	2662
				Examiner Name	GREGORY B. SEFCHECK
Sheet	1	of	2	Attorney Docket Number	MIPS.0164-01-US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-5708814	01-13-1998	SHORT ET AL.	
		US-6460105	10-01-2002	JONES ET AL.	
		US-20020049964	04-25-2002	TAKEYAMA ET AL.	
		US-20020071393	06-13-2002	ENRIQUE MUSOLL	
		US-4200927	04-29-1980	HUGHES ET AL.	
		US-6535905	03-18-2003	KALAFATIS ET AL.	
		US-20010052053	12-13-2001	NEMIROVSKY ET AL.	
		US-20020083173	06-27-2002	MUSOLL ET AL.	
		US Application Serial No. 09/608,750	Not Published	NEMIROVSKY ET AL.	
		US			
		US			
		US			

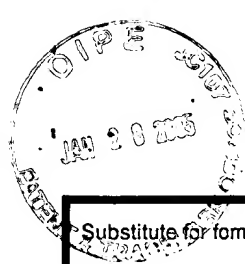
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	BA	WO-03/005645-A2	01-16-2003	SAMPATH ET AL.		

Examiner Signature		Date Considered	
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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				Group Art Unit	2662
Sheet	2	of	2	Examiner Name	GREGORY B. SEFCHECK
				Attorney Docket Number	MIPS.0164-01-US

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	AA	YAMAMOTO, WAYNE. <i>An Analysis of Multistreamed, Superscalar Processor Architectures</i> . University of California Santa Barbara Dissertation. December 1995. Santa Barbara, US.	
	AB	YAMAMOTO et al. "Increasing Superscalar Performance Through Multistreaming." <i>Parallel Architectures and Compilation Techniques (PACT '95)</i> . 1995	
	AC	The PowerPC Architecture: A Specification for a New Family of RISC Processors. 2 nd Ed. May 1994. pp. 70-72. Morgan Kaufmann. San Francisco, US.	
	AD	MC68020 32-Bit Microprocessor User's Manual. 3 rd Ed.. 1989. pp. 3-125, 3-126, and 3-127. Prentice Hall, NJ, US.	
	AE	POTEL, M. J. "Real-Time Playback in Animation Systems." <i>Proceedings of the 4th Annual Conference on Computer Graphics and Interactive Techniques</i> . 1977. pp. 72-77. San Jose, CA, US.	
	AF	ARM Architecture Reference Manual. 1996. pp. 3-41, 3-42, 3-43, 3-67, and 3-68. Prentice Hall, NJ, US.	
	AG	ESA/390 Principles of Operation. IBM Online Publications Center Reference Number SA22-7201-08. Table of Contents and paras. 7.5.31 and 7.5.70. IBM Corporation. Boulder, CO, US.	
	AH	MC88110 Second Generation RISC Microprocessor User's Manual. 1991. pp. 10-66, 10-67, and 10-71. Motorola, Inc.	
	AI	DIEFENDORFF, KEITH ET AL. "Organization of the Motorola 88110 Superscalar RISC Microprocessor." <i>IEEE Journal of Microelectronics</i> . April 1992. pp. 40-63. Vol. 12, No. 2. IEEE. New York, NY, US.	
	AJ	KANE, GERRY. <i>PA-RISC 2.0 Architecture</i> . 1996, pp. 7-106 and 7-107. Prentice Hall. NJ, US.	
	AK	DIEFENDORFF, KEITH ET AL. "Altivec Extension to PowerPC Accelerates Media Processing." <i>IEEE Journal of Microelectronics</i> . Vol. 20, No. 2 (2000): pp. 85-95	
	AL	GRUNEWALD, WINFRIED ET AL. "Towards Extremely Fast Context Switching in a Block Multithreaded Processor." <i>Proceedings of EUROMICRO 22</i> , 1996. pp. 592-599	
	AM	BRADFORD, JEFFREY ET AL. "Efficient Synchronization for Multithreaded Processors." <i>Workshop on Multithreaded Execution, Architecture, and Compilation</i> . Jan-Feb 1998. pp. 1-4	
	AN	PAI, VIJAY ET AL. "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors." <i>Proceedings of ASPLOS-VII</i> , Oct. 1996: pp. 12-23, ACM, Inc.	
	AO	YOAZ ET AL. "Speculation Techniques for Improving Load Related Instruction Scheduling." 1999. Pages 42-53, IEEE.	
	AP	KESSLER, R. E. "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz." August 1998.	
	AQ	DONALDSON ET AL. "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance." <i>26th Hawaii Conference on Systems Sciences</i> . Vol. 1. 1993. Pages 448-456.	
	AR	NEMIROVSKY ET AL. "DISC: Dynamic Instruction Stream Computer." ACM. 1991. Pages 163-171	
	AS	MELVIN ET AL., "Extended Instruction Set for a Packet Processing Applications," July 5, 2001, Disclosure Document #496559, USPTO	
	AT	SAMPATH ET AL., "Mechanism to Un-speculatively Pre-fetch Instructions from the Thread Associated to a Packet," April 2, 2001, Disclosure Document #491527, USPTO	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

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